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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/477,107	12/31/1999	CHRISTOPHER L. HAMLIN	K35A0576	8721

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WESTERN DIGITAL CORP.
20511 LAKE FOREST DRIVE
C205 - INTELLECTUAL PROPERTY DEPARTMENT
LAKE FOREST, CA 92630

EXAMINER	
DADA, BEEMNET W	

ART UNIT	PAPER NUMBER
2135	7

DATE MAILED: 04/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/477,107	HAMLIN, CHRISTOPHER L.	
	Examiner	Art Unit	
	Beemnet W Dada	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-8, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (hereinafter refereed to as Brown) (U.S. Patent No. 5,892,826) in view of Lewis (U.S. Patent No. 5,734,819).

3. As per claims 1 and 8, Brown teaches an integrated circuit for selectively encrypting plaintext data received form a first device to produce encrypted data to send to a second device (column 6, claim 1), the integrated circuit comprising:

controllable encryption circuitry (figure 1-2, unit 60) comprising:

a data input (i.e. terminal coupled to internal data bus for providing plaintext data) (column 6, lines 14-15 and figure 1-2);

an enable input (i.e. control input) (column 6, lines 16-17 and figure 1-2, bypass signal input);

a data output (i.e. terminal coupled to external data bus for providing encrypted data) (column 6, lines 15-16, and figure 1-2);

an encryption determination circuit , responsive to internal address signal, for producing a first verification signal for use in controlling the enable input of the encryption circuitry to enable the encryption circuitry to provide the encrypted data via the encrypted text output (column 3, lines15-28).

Furthermore, Brown teaches an expanded mode of operation (i.e. address space divided in internal and external memory portions), partitioning the address space to allow certain input/output peripherals or memory devices to be accessed with clear text (column 2, lines 30-42), implementing encryption based on the address at which the data is located (i.e. as understood by the examiner indirectly verifying whether a device is internal or external device) (column 4, lines 16-17), and generating an address signal corresponding to different combinations of the address space and selectively performing encryption based on the signal (column 3, lines 15-28).

Brown does not explicitly teach a method of authenticating a device. However, Lewis teaches a method of authenticating a device using unique chip identifier (column 2, lines 21-34). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement a method of device authentication using chip identifier thought by Lewis into the verification based on an address where data is located thought by Brown, because such method prevents software program from executing on unlicensed computer system and further improves the security of the system from cryptanalysis attacks.

4. As per claims 3 and 10, the combination of Brown and Lewis teaches an integrated circuit for selectively encrypting plaintext data received form a first device to produce encrypted data to send to a second device as applied to claims 1 and 8 above. Furthermore, Lewis teaches authentication (verification) of a device using a device identifier by comparing the device identifier to a corresponding expected device identifier (column 2, lines 21-34).

5. As per claims 4 and 11, the combination of Brown and Lewis teaches the integrated circuit as applied to claims 3 and 10 above. Furthermore, Lewis teaches a method of hardwiring a chip identifier (column 1, lines 45-60).

6. As per claims 5 and 12, the combination of Brown and Lewis teaches the integrated circuit as applied to claims 3 and 10 above. Furthermore, Lewis teaches, at column 1, lines 27-35, method of storing device identifier in a non-volatile memory.

7. As per claims 6 and 13, the combination of Brown and Lewis teaches the integrated circuit as applied to claims 1 and 8 above. Furthermore, Lewis teaches, at column 2, lines 7-49, a method of generating message authentication code over text data received from a device using a secret key and verifying the device by verifying the message authentication code using a secret key.

8. As per claims 7 and 14, the combination of Brown and Lewis teaches an integrated circuit as applied to claims 1 and 8 above. Furthermore, Lewis teaches, at column 1, lines 27-35, a non-volatile memory used for storing device identifier.

9. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown in view Lewis as applied to claims 1 and 8 above and further in view of Le Rue (U.S. Patent No. 5,694,469).

10. As per claims 2 and 9, the combination of Brown and Lewis teaches an integrated circuit as applied to claims 1 and 8 above. Furthermore, Brown shows, at column 3, lines 15-36, an encryption determination circuit having an input terminal for receiving signal for validating a device; an output terminal for providing a bypass signal (verification signal) to the encryption circuitry allowing the encryption circuitry to provide encryption. The combination of Brown and Lewis does not teach two encryption determination circuits used together to verify both the source and the destination devices. However, Le Rue teaches, at column 4, lines 37-48, a method of verifying the source device and destination device before allowing process to continue, thereby teaching an enhancement of the authentication process. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Le Rue related to authentication the source and destination devices and have modified the integrated circuit of Brown and Lewis. One would have been motivated to make such a modification in view of the suggestion in Le Rue that the

security of the system would be further enhanced by the fact that access is made based on authentication of both the source and destination devices. Therefore it would have been obvious to employ the teachings of Le Rue within the combination of Brown and Le Rue to obtain the claimed invention.

Response to Arguments

11. Applicant's arguments with respect to claims 1, 3, 8 and 10 have been considered but are moot in view of the new ground(s) of rejection. *See Claim rejections under 35 USC 103 (a) [Brown in view of Lewis] above.*

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Beemnet W Dada whose telephone number is (703) 305-8895. The examiner can normally be reached on Monday - Friday (8:30 am - 6:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on (703) 305-4393. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Beemnet Dada

March 25, 2004